

## MODULE DESCRIPTION FORM

## نموذج وصف المادة الدراسية

Module Information			
معلومات المادة الدراسية			
Module Title	Digital Fundamentals		Module Delivery
Module Type	Core		✓ Theory Lecture ✓ Lab Tutorial Practical Seminar
Module Code	CET1101		
ECTS Credits	6		
SWL (hr/sem)	150		
Module Level	1	Semester of Delivery	
Administering Department	CET	College	BCESU
Module Leader	Mohammed jaffr ali	e-mail	<a href="mailto:Mohammedjaffar@baghdadcollege.edu.iq">Mohammedjaffar@baghdadcollege.edu.iq</a>
Module Leader's Acad. Title	Ass.lecturer	Module Leader's Qualification	Msc.
Module Tutor	Rafal Nasser Taqi	e-mail	<a href="mailto:rafal2023@baghdadcollege.edu.iq">rafal2023@baghdadcollege.edu.iq</a>
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Scientific Committee Approval Date	31/12/2023	Version Number	1.0

Relation with other Modules			
العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	Semester	
Co-requisites module	None	Semester	

<b>Module Aims, Learning Outcomes and Indicative Contents</b> <b>أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية</b>	
<b>Module Aims</b> <b>أهداف المادة الدراسية</b>	<ol style="list-style-type: none"> <li>1. To be able to deal with the number systems and codes.</li> <li>2. To understand the functionality of logic gates.</li> <li>3. To have a skill to use the logic gates in designing logic circuit.</li> <li>4. To have a skill to simplify the digital circuits.</li> <li>5. To learn the simplification process, Boolean expression, Demorgans law, and Karnaugh map..</li> <li>6. To understand the principles for designing logic circuit.</li> <li>7. To understand adder, subtractor, decoder, incoder, multiplexer, demultipleaer, and comparator circuits.</li> </ol>
<b>Module Learning Outcomes</b> <b>مخرجات التعلم للمادة الدراسية</b>	<ol style="list-style-type: none"> <li>1. Recognize each type of number systems.</li> <li>2. Identify the process of converting between number systems.</li> <li>3. Summarize the types of logic gates.</li> <li>4. Discuss the use of each gate.</li> <li>5. Describe design of logic circuit by using logic gats.</li> <li>6. Explain the simplification processes.</li> <li>7. Explain Boolean expression and Demorgan's law.</li> <li>8. Explain the Karnaugh map for different numbers of bits.</li> <li>9. Discuss the design of logic circuit before and after simplification.</li> <li>10. Explain the combinational logic circuit.</li> <li>11. Identify the adder, subtractor, decoder, encoder, multiplexer, demultiplexer, comparator circuits, and code conversion.</li> <li>12. Identify the basic circuit elements and their applications</li> </ol>
<b>Indicative Contents</b> <b>المحتويات الإرشادية</b>	<p>Indicative content includes the following.</p> <p>--Number systems - decimal, binary, octal, and hexadecimal number system, conversion, operation. <b>[8 hrs]</b></p> <p>-Codes- excess-3,gray code, conversions, operations, complements <b>[8 hrs]</b></p> <p>--Logic gates-NOT, AND, OR, NOR, NAND, XOR, XNOR. <b>[5 hrs]</b></p> <p>--Logic simplification-Boolean theorem and Demorgans law. <b>[10 hrs]</b></p> <p>--Karnaugh map-SOP, POS, and don't care. <b>[10 hrs]</b></p> <p>--Arithmetic operations Part A- adder, parallel binary adder, subtractor, adder-subtractor <b>[10 hrs]</b></p> <p>--Arithmetic operations Part B- multiplexer, demultiplexer, decoder, encoder, comparator, and code conversion. <b>[10 hrs]</b></p>

**Learning and Teaching Strategies**

## استراتيجيات التعلم والتعليم

<b>Strategies</b>	Type something like: The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering type of simple experiments involving some sampling activities that are interesting to the students.
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**Student Workload (SWL)**

## الحمل الدراسي للطالب موزع على 15 اسبوع

<b>Structured SWL (h/sem)</b> الحمل الدراسي المنتظم للطالب خلال الفصل	64	<b>Structured SWL (h/w)</b> الحمل الدراسي المنتظم للطالب أسبوعياً	4.26
<b>Unstructured SWL (h/sem)</b> الحمل الدراسي غير المنتظم للطالب خلال الفصل	86	<b>Unstructured SWL (h/w)</b> الحمل الدراسي غير المنتظم للطالب أسبوعياً	5.73
<b>Total SWL (h/sem)</b> الحمل الدراسي الكلي للطالب خلال الفصل	150		

**Module Evaluation**

## تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
<b>Formative assessment</b>	<b>Quiz</b>	2	10% (10)	5, 10	LO #1- 3, LO # 4 - 8
	<b>Assignments</b>	1	10% (10)	12	LO # 1-11
	<b>Projects / Lab.</b>	1	10% (10)	Continuous	LO # 1-12
	<b>Report</b>	1	10% (10)	Continuous	LO # 1-12
<b>Summative assessment</b>	<b>Midterm Exam</b>	2 hr	10% (10)	10	LO # 1-10
	<b>Final Exam</b>	4hr	50% (50)	16	All
<b>Total assessment</b>			100% (100 Marks)		

**Delivery Plan (Weekly Syllabus)**

## المنهاج الاسبوعي النظري

	<b>Material Covered</b>
<b>Week 1</b>	Number systems (decimal, binary, octal, conversions, operations)
<b>Week 2</b>	Number systems (hexadecimal, BCD, conversions, operations)
<b>Week 3</b>	Number systems (excess-3, gray code, conversions, operations, complements)
<b>Week 4</b>	Logic gates (AND, OR, NOT, NAND, NOR, XOR, XNOR)
<b>Week 5</b>	Logic simplification (Boolean theorem)
<b>Week 6</b>	Logic simplification (Demorgan's theorem)
<b>Week 7</b>	Karnaugh maps ( 2-variables, 3-variables, )
<b>Week 8</b>	Karnaugh maps (4-variables (SOP, POS, don't care))
<b>Week 9</b>	Karnaugh maps (5-variables, (SOP, POS, don't care))
<b>Week 10</b>	Midterm exam
<b>Week 11</b>	Arithmetic operations
<b>Week 12</b>	Arithmetic operations (decoder, encoder)
<b>Week 13</b>	Arithmetic operations (Multiplexer, Demultiplexer)
<b>Week 14</b>	Arithmetic operations (comparators)
<b>Week 15</b>	Arithmetic operations (code conversion)
<b>Week 16</b>	<b>Preparatory week before the final Exam</b>

**Delivery Plan (Weekly Lab. Syllabus)**

المنهاج الاسبوعي للمختبر

	Material Covered
<b>Week 1</b>	logic gates (NOT, AND,OR)
<b>Week 2</b>	Logic gates (NOR.NAND)
<b>Week 3</b>	Logic gates (XOR,XNOR)
<b>Week 4</b>	Boolean theorem
<b>Week 5</b>	Demorgan's law
<b>Week 6</b>	Karnaugh map
<b>Week 7</b>	SOP
<b>Week 8</b>	POS, don't care
<b>Week 9</b>	Combinational circuit (half adder, full adder)
<b>Week 10</b>	Combinational circuit (Half subtractor, full subtractor)
<b>Week 11</b>	Decoder and Encoder circuits
<b>Week 12</b>	Multiplexer and Demultiplexer circuits
<b>Week 13</b>	Comparator circuit
<b>Week 14</b>	Code conversion circuits

**Learning and Teaching Resources**

مصادر التعلم والتدريس

	Text	Available in the Library?
<b>Required Texts</b>	Digital Fundamentals by Floyed	Yes
<b>Recommended Texts</b>	Digital circuit analysis and design with Simulink modeling by Steven T. Karris	No
<b>Websites</b>		

Grading Scheme مخطط الدرجات				
Group	Grade	التقدير	Marks (%)	Definition
<b>Success Group (50 - 100)</b>	<b>A</b> - Excellent	امتياز	90 - 100	Outstanding Performance
	<b>B</b> - Very Good	جيد جدا	80 - 89	Above average with some errors
	<b>C</b> - Good	جيد	70 - 79	Sound work with notable errors
	<b>D</b> - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	<b>E</b> - Sufficient	مقبول	50 - 59	Work meets minimum criteria
<b>Fail Group (0 – 49)</b>	<b>FX</b> – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	<b>F</b> – Fail	راسب	(0-44)	Considerable amount of work required
<b>Note:</b> Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.				